Low Dropout Regulator Design

Error Amplifier Design

The schematic for our error amplifier is seen in Figure 1. The error amplifier was a high-swing folded cascode with NMOS inputs. The folded-cascode was chosen because it has a high gain and large bandwidth. The PMOS high-swing was implemented to maintain a good output swing range, although having a diode-tied PMOS current mirror, with certain adjustments, could have sufficed. The high-swing cascode was implemented on the PMOS current mirror. A poor PSR (around 0 dB) was desired for the EA in order for most of the signal to reach the pass device (the PMOS output). Adding the pass device at the output makes the PSR of the LDO really low (less than -50 dB) for most frequencies.

The error amplifier was initially designed to operate under $\Delta = 0.1$V. The biasing current was chosen to be $10\mu A$ for multiple reasons, one of them being a less undershoot in the transient response. For a 1.3V output and a transient response with a 1 mA to 20 mA step, a $10\mu A$ bias current yielded 31.2% undershoot while a test using a $100\mu A$ bias current had a 36.8% undershoot. A $10\mu A$ bias current also did not waste as much current through the error amplifier. The benefit of a larger current source is that it makes it easier to achieve a stable LDO for all load currents, however, minimizing the current going through the EA, and thus the quiscient current, was a desired specification for our LDO design.

LDO Design and Tradeoffs

The error amplifier provided a gain of 60 dB and had a unity gain frequency of 4.15 MHz at a 0.1 mA load current and 4.54 MHz at 30 mA. A high gain helped with meeting the load and line regulation requirements. Equations 1 and 2 below show how important high gain is for achieving proper line and load regulation:

$$L_{DR} \approx \frac{rds_p||(R_{F1} + R_{F2})}{1 + \beta A_{EA0} \cdot gm_p \cdot [rds_p||(R_{F1} + R_{F2})]} \tag{1}$$

$$L_R \approx \frac{1}{\beta A_{EA0}} \tag{2}$$

where $\beta = \frac{1}{2}$ because the resistors had a $1:1$ ratio. For a desired output voltage of 1.3V, V_{REF} was chosen to be around 0.65V because $V_{OUT} \approx \frac{V_{REF}}{\beta} \approx 1.3V$.

The output of the EA was a PMOS for a better PSR response (the gate of the transistor is not coupled to the supply voltage and thus it behaves as a common-gate stage amplifier with extremely low gain). This causes a high output impedance, which improves the load regulation of the LDO. The PSR requirement was more difficult to meet at higher frequencies when the load current was low; we did not meet the $-20dB$ PSR at 1MHz specification for a 0.1 mA load current, for example (although we got close with $\approx -15dB$). The peak in the PSR response is due to a zero at the output of the EA (located after the 1 MHz mark in our case). Shifting the pole at the output of the LDO to a lower frequency and making it dominant (by adding a large capacitance at the output or a large capacitance between V_{IN} and the output of the EA) would have removed this peak in PSR and improved it significantly.

As for choosing the resistor values (while maintaining the $1:1$ ratio), it came down to finding the ones that delivered most of the current from the source to the load, rather than to the amplifier. Lower resistance values can help achieve stability for lower load currents because the pole at the output gets pushed to even higher frequencies. The downside of

this is that the quiscient current becomes quite high. Therefore, high resistor values were selected: $100k\Omega$ for both feedback resistors. This ensured that almost all of the current was delivered to the load, but left us with the issue of good stability (or phase margins greater than 45 degrees) to deal with next.

The most challenging part of the LDO design was maintaining a good phase margin for all load currents (and thus good transient responses). The dominant pole of the LDO was at the output of the EA: the high output impedance of the EA and high gate-to-source capacitance of the output PMOS caused a pole at a low frequency (around 1-2 kHz). The impedance could have been decreased by using a buffer but that's about it as far as shifting that pole. As for the output pole, we decided that it was best for it to occur at a much higher frequency. This ensures a good phase margin for all load currents (0.1 mA to 30 mA). Changing the feedback resistances was ruled out in the analysis regarding quiscient current above. Thus, the output capicitance was chosen to be low to push the output pole to much higher frequencies. The output capacitance value that produced stable outputs for all load currents was 50pF.

The main drawback that this had was on the undershoot of the transient response. A smaller capacitance causes a very large change in output voltage (due to the charging and discharing of the capacitor) when tested with the current steps in the transient response simulation. An even lower capacitance would have improved the phase margin for lower load currents even more, but the undershoot would have been even worse. Therefore, a 50 pF capacitor sufficed for our design. This did yield a quicker settling time back to 1.3V, however (we achieved a worst-case settling time of 260ns). In the end, the phase margin was less than 45 degrees only for a load current of 0.1 mA (around 37 degrees); any load current greater than and including 0.2 mA had a phase margin greater than 45 degrees. This could have been fixed by decreasing the output capacitance even more for the cost of a worse undershoot.

Since the amplifier schematic does not state it, the PMOS transistor at the output had a 1mm width and 180nm length. The standard transistor size for the EA was a 2.16nm width and a 540nm length, as indicated in Table 1 below.

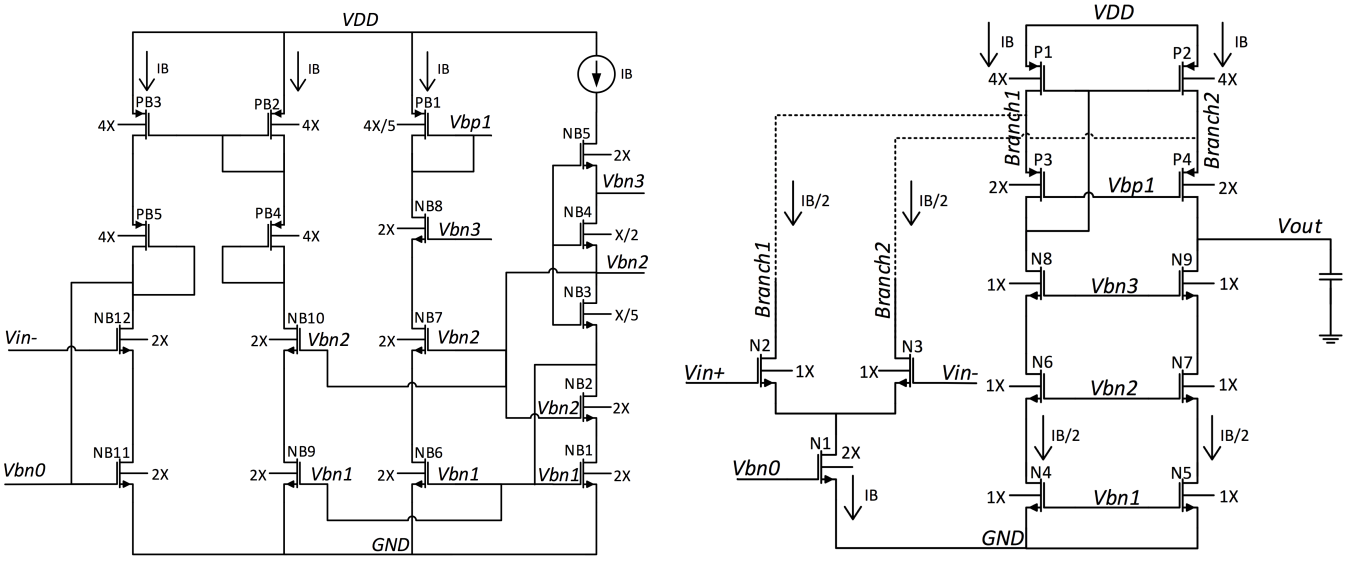


Figure 1: Error Amplifier Schematic - Folded Cascode (Right) and Biasing Network (Left)

Table 1: Parameters of EA Transistors - Folded Cascode (Left) and Biasing Network (Right)

Transistor	Size (X$\times\frac{2.16nm}{540nm}$)	Bias Current (μA)	$gm\,(\frac{\mu}{\Omega})$	Δ (mV)
N1	2X	10.09	159.5	103.2
N2	1X	5.045	85.17	92.04
N3	1X	5.045	85.17	92.04
N4	1X	4.929	75.73	103.7
N5	1X	4.929	75.73	103.7
N6	1X	4.929	75.73	101.1
N7	1X	4.929	75.73	101.1
N8	1X	4.929	84.23	90.20
N9	1X	4.929	84.23	90.20
P1	4X	-9.974	120.2	-140.0
P2	4X	-9.974	120.2	-140.0
P3	2X	-4.929	64.55	-148.6
P4	2X	-4.929	64.55	-148.6

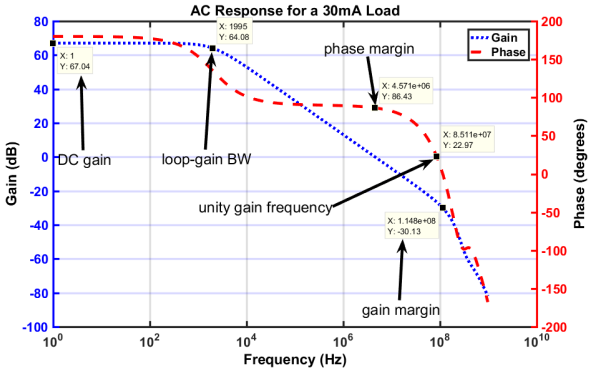
(Note: * denotes transistors in triode; all the others are in saturation. All the PMOS transistors' body terminals were tied to the power supply and all the NMOS transistors' body terminals were tied to ground.)

Transistor	Size (X$\times\frac{2.16nm}{540nm}$)	Bias Current (μA)	$gm\,(\frac{\mu}{\Omega})$	Δ (mV)
NB1	2X	10.00	155.3	103.7
NB2	2X	10.00	169.0	95.05
NB3*	0.2X	10.00	32.00	377.8
NB4*	0.5X	10.00	66.11	216.5
NB5	2X	10.00	174.0	82.26
NB6	2X	9.86	151.4	103.7
NB7	2X	9.86	150.8	101.2
NB8	2X	9.86	168.4	90.51
NB9	2X	9.99	155.2	103.7
NB10	2X	9.99	168.8	95.19
NB11	2X	9.96	156.0	103.2
NB12	2X	9.96	168.6	94.76
PB1	0.8X	-9.855	57.13	-329.7
PB2	4X	-9.994	130.9	-141.6
PB3	4X	-9.963	130.6	-141.6
PB4	4X	-9.994	129	-137
PB5	4X	-9.963	128.9	-136.8

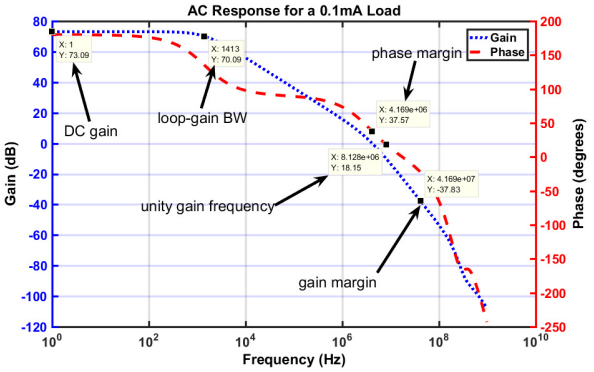
Table 2: Performance Summary

Design parameter/variable	Simulated performance	Specification
Input voltage (V_{IN})	1.6V – 2V	1.6V – 2V
Output voltage (V_{OUT})	1.2V – 1.4V	1.2V – 1.4V
Total capacitance	50 pF	$\leq$ 500 pF
Output voltage error	$\leq$ 0.053%	$\leq \pm$3%
Load currents	0.1mA – 30mA	0.1mA – 30mA
Load currents with PM $\geq 45°$	0.2mA – 30mA	–
DC load regulation	$\leq 36\mu$V/mA	$\leq 100\mu$V/mA
DC line regulation	$\leq$ 0.5mV/V	$\leq$ 2mV/V
Quiescent current (I_L = 0.1mA/30mA)	66.30μA/66.35μA	Minimum
Current efficiency (I_L = 0.1mA/30mA)	60.10%/99.8%	–
PSR: V_{IN}/V_{OUT} = 1.8V/1.3V $I_L = 30mA$ (@1KHz/1MHz)	-78.1dB/-30.3dB	-40dB/-20dB
PSR: V_{IN}/V_{OUT} = 1.65V/1.4V $I_L = 30mA$ (@1KHz/1MHz)	-59.2dB/-17.1dB	-40dB/-20dB

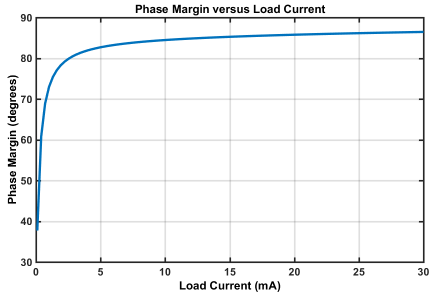
Design parameter/variable	Simulated performance	Specification
Worst-case PSR	-0.0375dB	–
DC loop gain: V_{IN}/V_{OUT} = 1.8V/1.3V (I_L = 0.1mA/30mA)	73.09dB/67.04dB	–
DC loop gain: V_{IN}/V_{OUT} = 1.6V/1.4V (I_L = 0.1mA/30mA)	73.07dB/50.81dB	–
Worst-case DC loop gain	50.81dB	–
Loop-gain unity gain frequency (I_L = 0.1mA/30mA)	4.15MHz/4.54MHz	–
Loop-gain phase margin (I_L = 0.1mA/0.2mA/30mA)	37.73°/49.03°/86.46°	–
Loop-gain gain margin (I_L = 0.1mA/30mA)	22.74dB/30.03dB	–
Transient response undershoot/settling time (1mA to 30mA step)	44.92%/0.20μs	Undershoot $\leq$ 1%
Transient response overshoot/settling time (30mA to 1mA step)	28.21%/0.26μs	–
Output noise (I_L = 0.1mA/I_L = 30mA)	320 $\frac{pV^2}{Hz}$/318 $\frac{pV^2}{Hz}$	–



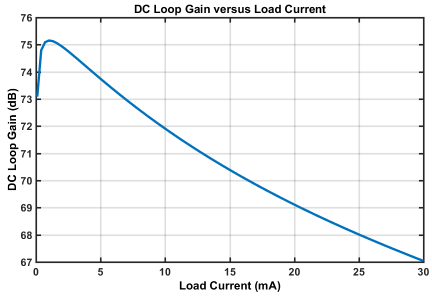
(a) Plot 3.1a - AC Response ($I_L = 30$ mA)



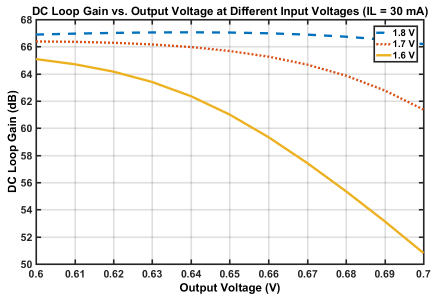
(b) Plot 3.1b - AC Response ($I_L = 0.1$ mA)



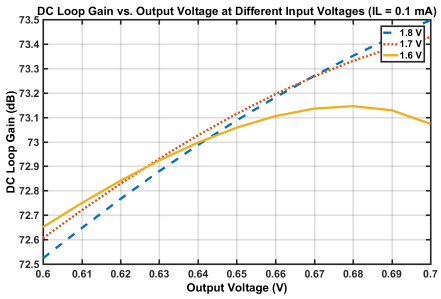
(a) Plot 3.2 - Phase Margin vs. I_L



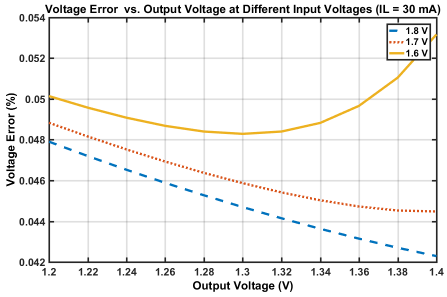
(b) Plot 3.3 - DC Loop Gain vs. I_L



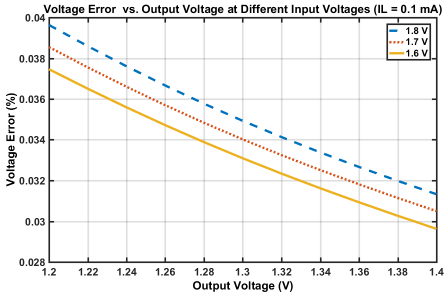
(a) Plot 3.4A - DC Loop Gain vs. Output Voltage ($I_L = 30$ mA)



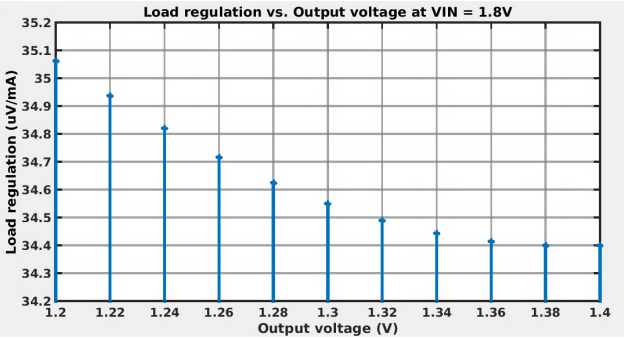
(b) Plot 3.4A - DC Loop Gain vs. Output Voltage ($I_L = 0.1$ mA)



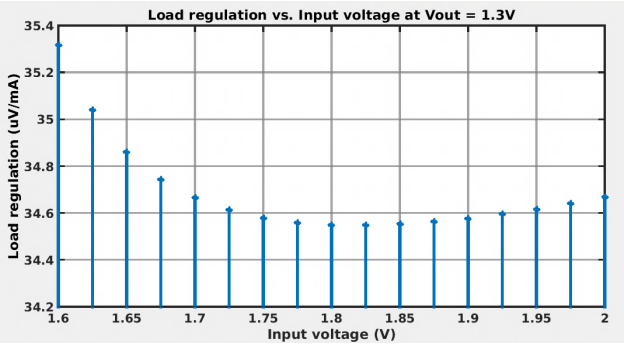
(c) Plot 3.4B - Voltage Error % vs. Output Voltage ($I_L = 30$ mA)



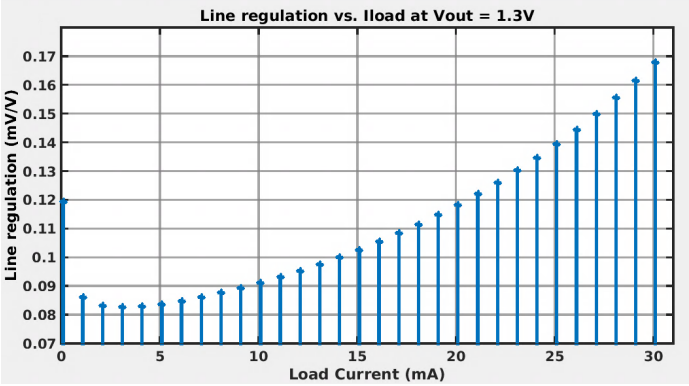
(d) Plot 3.4B - Voltage Error % vs. Output Voltage($I_L = 0.1$ mA)



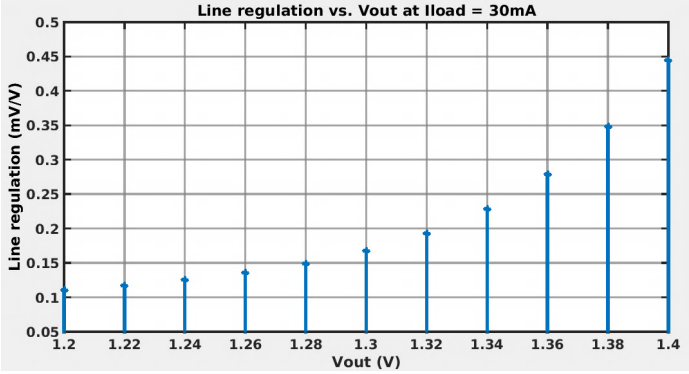
(a) Plot 4.1 - Load Regulation vs. Output Voltage at $V_{IN} = 1.8V$



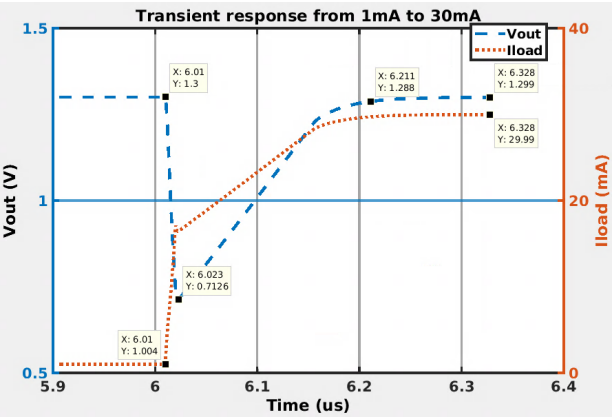
(b) Plot 4.2 - Load Regulation vs. Input Voltage at $V_{OUT} = 1.3V$



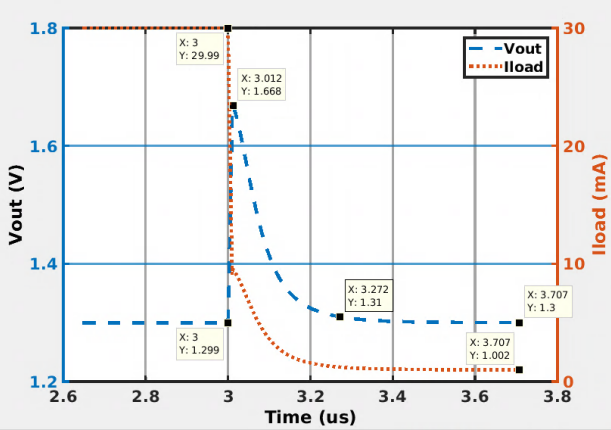
(a) Plot 4.3 - Line Regulation vs. Load Current at $V_{OUT} = 1.3V$



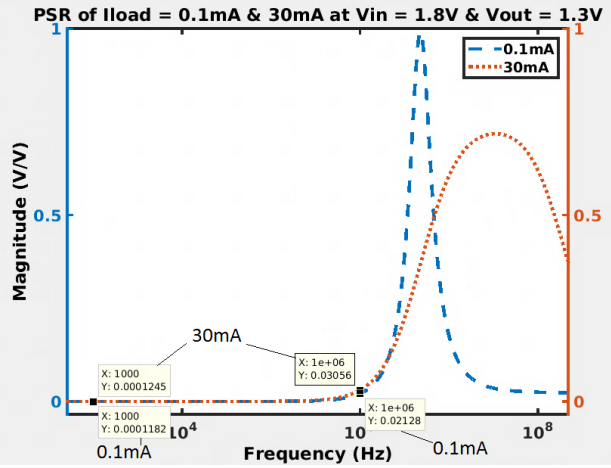
(b) Plot 4.4 - Line Regulation vs. Output Voltage at $I_L = 30$ mA



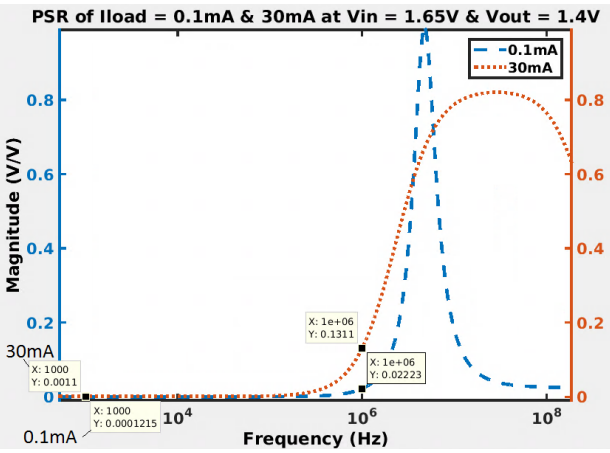
(a) Plot 5.1a - Transient Response (1mA to 30mA step)



(b) Plot 5.1a - Transient Response (30mA to 1mA step)



(a) Plot 5.2a - PSR at 0.1mA and 30mA for $V_{IN}/V_{OUT} = 1.8V/1.3V$



(b) Plot 5.2b - PSR at 0.1mA and 30mA for $V_{IN}/V_{OUT} = 1.65V/1.4V$