Project 1 - Impedance Matching Network

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Background

The goal of this project was to create an impedance matching network that matched a 200 ohm load to a 50 ohm system with a return loss more than 20 dB over a 40% fractional bandwidth and a 2 GHz center frequency. The substrate specified was Rogers 5880 HH with a top/bottom copper cladding of 17 micrometers, dielectric constant of 2.2, and a dielectric thickness of 0.062 inches. The load was to be attached through a via at the end of our matching network, with the other end connecting to an SMA connector on a testing unit where the measurements were performed.

Design Process

The transformation from 200 ohms to 50 ohms was done using multiple quarter-wave transformers. One quarter-wave transformer would not yield the desired bandwidth. When splitting this design into two transformers, with an intermediate impedance of 100 ohms (the geometrical mean of 200 and 50), the bandwidth was sufficient but it was not safe enough to call it a day (just barely above 40%). Therefore, two intermediate impedances were chosen and three quarter-wave transformers were designed. Using the equation for input impedance seen at a quarter-wave transformer seen below:

$$Z_{in} = \frac{Z_0^2}{Z_L} \tag{1}$$

The characteristic impedances of the microstrips were determined. The two intermediate impedances were chosen to be 100 ohms and 70.69 ohms (the geometric mean between 100 and 50). The reason the second intermediate impedance was not chosen to between the 100 and 200 ohm resistances was because the line between the intermediate impedance and the 200 ohm termination would need a line thinner than the allowed requirement of 0.25 mm. The line impedances were calculated to be:

$$Z_{in,1} = \frac{Z_0^2}{Z_L} = 100 = \frac{Z_0^2}{200} \rightarrow Z_{0,1} = 141.42\,ohms \tag{2}$$

$$Z_{in,2} = \frac{Z_0^2}{Z_L} = 70.69 = \frac{Z_0^2}{100} \rightarrow Z_{0,2} = 84.08\,ohms \tag{3}$$

$$Z_{in,3} = \frac{Z_0^2}{Z_L} = 50 = \frac{Z_0^2}{70.69} \rightarrow Z_{0,3} = 59.45\,ohms \tag{4}$$

Moving from the 50 ohm system to the 200 ohm load, we would therefore have a line with impedance 59.45 ohms, a line with 84.08 ohms, and a line with 141.42 ohms, in that order. Using the LineCalc and by entering the characteristics of the substrate given above, the lengths and widths of these lines were calculated. Note that the width of the line decreases as its characteristic impedance increases.

Next, the board layout was genered. To fit the desired test unit dimensions of 1.25 inches by 1.5 inches, some meandering needed to be done. Some bends were added to properly do this. One bend was placed between the 59.45 ohm line and the 84.08 ohm line. This bend was given the same width of the 59.45 ohm line: 145.06 mils. The second bend was placed between the 84.08 ohm and 141.42 ohm lines. Through trial-and-error, this was given a width of 48.25 mils. Finally, one last bend was used to split the 141.42 ohm line in order to fit it into the desired dimensions. This was split into a line of lengths 700 mil and 229 mil (with the bend having the same width of 21.51 mil as both lines). This was essentially a series of trial-and-errors, where we tried several things like changing the widths of the bends, moving the bends around, different meanderings, etc. Eventually, the layout seen below was chosen since it matched the design specifications best. The resulting schematic and board layout are seen in Figures 1 and 2 below.

From LineCalc tool, the total loss for the whole matching network was determined to be 0.039 dB. This was done by adding the attenuation calculated from each microstrip in the network.

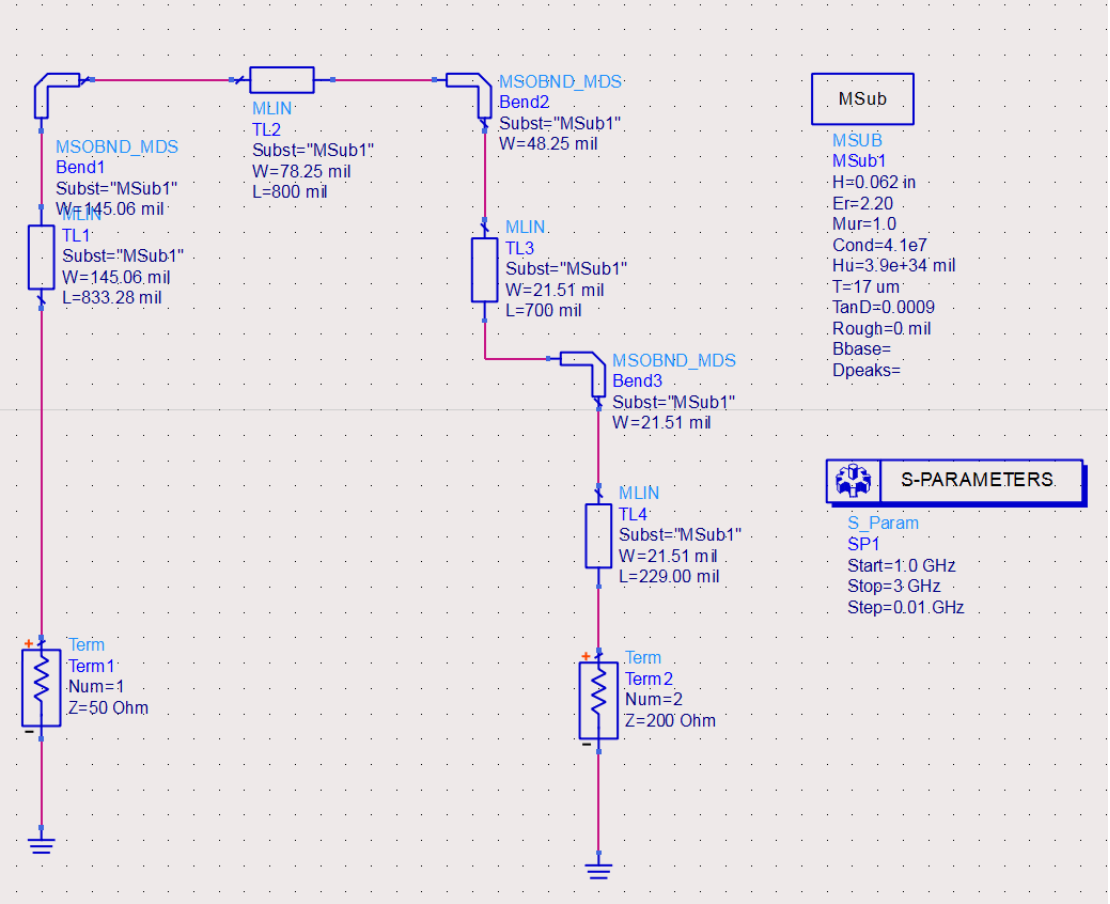

Figure 1: ADS Schematic with a S-parameter sweep from 1 GHz to 3 GHz

Results

The simulation results from the ADS schematic are seen below (Figure 3). As expected from a matching network, the return loss should be high (equivalent to a low S_{11} or S_{22} response) and the S_{21} and S_{12} plots should be close to 0 dB around the center frequency. The schematic results matched these expectations and the desired result of 20 dB or higher return loss (-20 dB or less S_{11}) over a 40% fractional bandwidth. The fractional bandwidth was calculated to be:

$$\frac{2.660\,GHz - 1.390\,GHz}{2\,GHz} = 63.5\% \tag{5}$$

The simulation from the board layout should have slightly worse results, since it takes into consideration the effects of meandering and coupling from the how the wires are placed. The results for the board layout simulations are seen below in Figure 4, and fortunately enough, the still meet the design requirement:

$$\frac{2.464\,GHz - 1.354\,GHz}{2\,GHz} = 55.5\% \tag{6}$$

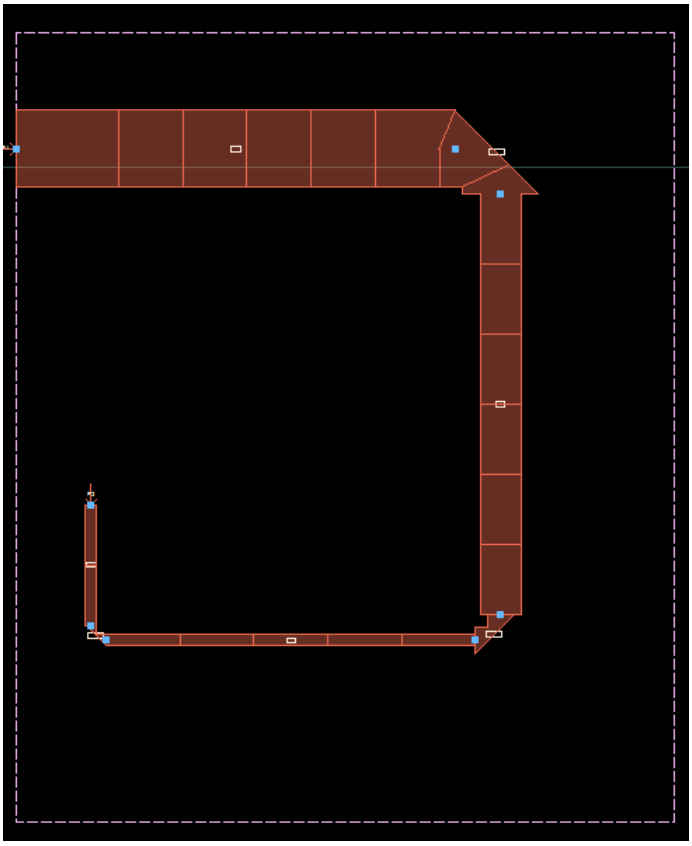

Figure 2: Board Layout

The results obtained from the actual measurement of the board, unfortunately, did not meet the design requirement. As it is our first design using Momentum, a lot of unexpected errors came up when the board was actually made. The calibration probably contributed the most to these errors, as the SMA connector and solder were not part of our simulations. The calibration kit itself was reportedly slightly damaged so that might also contribute to these inaccurare results. The switch from a Momentum simulation to a real-life measurement, in my opinion, is what could have caused these inaccuracies. Doing the measurement with a proper calibration is already hard enough on its own, and as with every application in design, the actual measurements are never identical to the simulated results. The measured data was plotted by attaching a 50-ohm termination to the input of a 1-port Data Item and grounding the reference port. For some odd reason, the generated plot was flipped and the -dB plot (not the dB plot) had to be plotted to obtain the S_{11} plot seen in Figure 6 below. The bandwidth is calculated to be:

$$\frac{2.204\,GHz - 2.115\,GHz}{2\,GHz} = 4.45\% \tag{7}$$

This is quite far from the design requirement, unfortunately. The causes of error discussed above help explain what could have gone wrong. Next time, however, these errors should be taken into account even more in our design process.

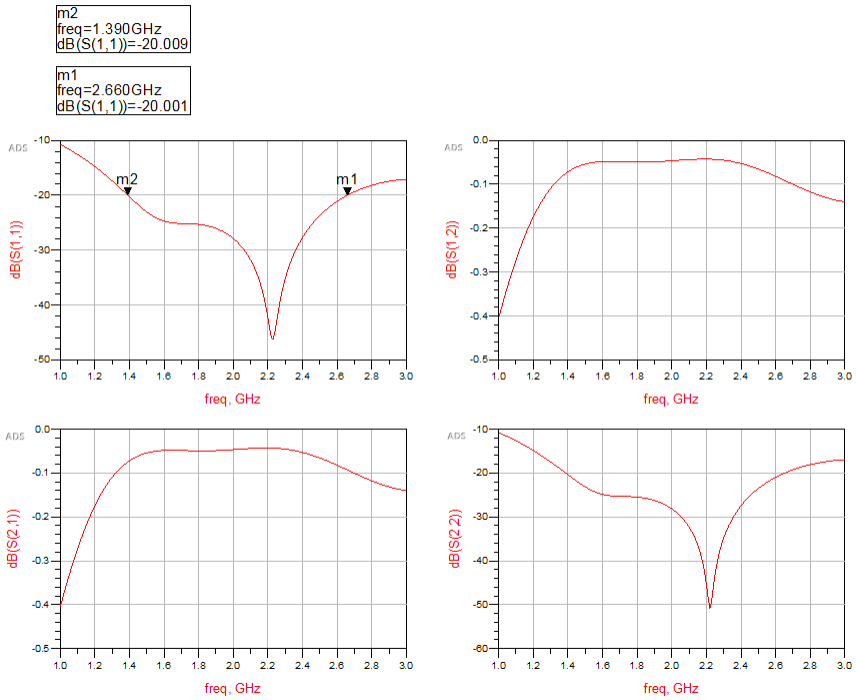

Figure 3: ADS Schematic Simulation Results

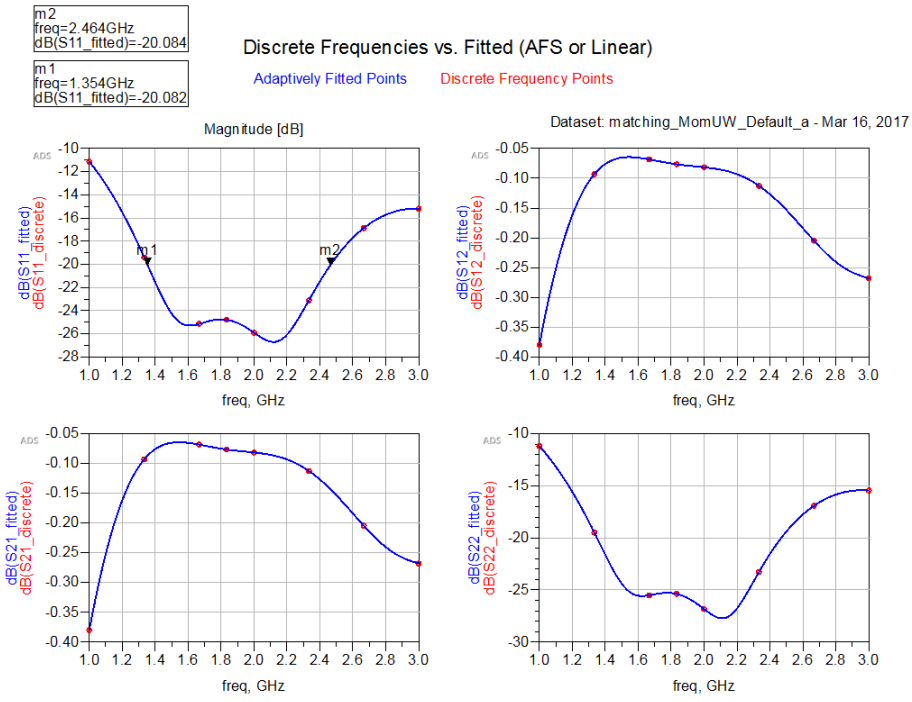

Figure 4: Board Layout Simulation Results

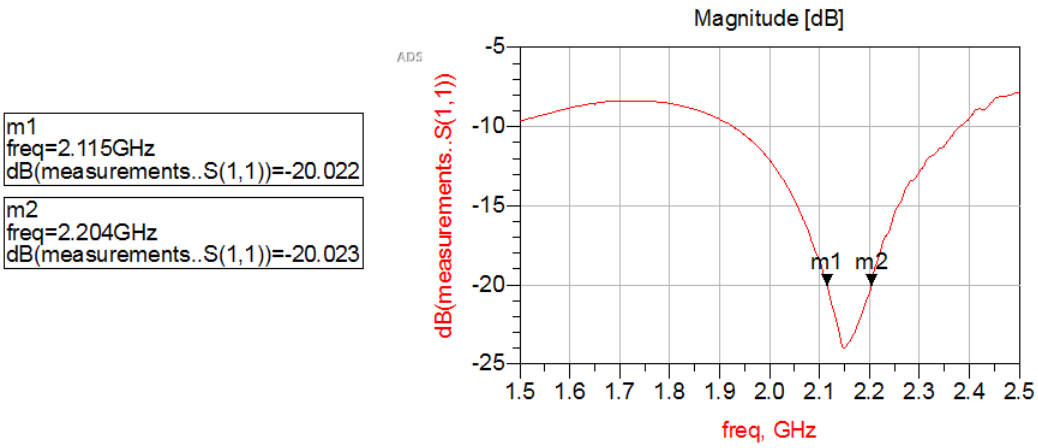

Figure 5: Measurement S11 Results